AUSTRALIAN RAIL TRACK CORPORATION LTD

Discipline: Engineering (Signalling) **Category: Standard**

Microlok II Design

ESD-05-12

Applicability

ARTC Network Wide	✓	**CRIA (NSW CRN)**	✓

Primary Source

SCP 23

Document Status

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1.3	13 August 2010	Standards	Manager Standards	Exec Manager SS&P 25/06/2010	CEO

Amendment Record

Version	Date Reviewed	Clause	Description of Amendment
1.0	9 April 09		First issue. Supersedes NSW Standard SCP 23 v1.3 Sections 2 and 3 only
1.1	7 October 2009		Disclaimer updated as per Risk & Safety Committee 14/09/2009
1.2	25 June 2010		Residual NSW standard SCP 23 retained. ESD-05-12 partially supersedes SCP 23.
1.3	13 August 2010	All	Issued as final.

Contents

1 Introduction

This policy details the process that shall be be followed when carrying out design activities for Microlok II applications for ARTC infrastructure.

2 Reference Documents

The following documents provide supporting information:

Ansaldo Documents

Microlok II System Description	SM-6800A
Microlok II Hardware Installation	SM-6800B
Microlok II System Start Up, Trouble Shooting & Maintenance	SM-6800C
Microlok II System Application Logic Programming Guide	SM 6800D
Microlok II Programmable Controller Platform Safety Application Issues	
Microlok II Application Logic Comparison Tool	SM-8584
Microlok, Microtrax, Genisys – Circuit design Application Notes	

ARTC Documents

Microlok Data Design Records	ESD-05-11
Design of Microlok II Interlockings	SCP 23 (NSW only)

3 System Configuration

3.1 General

This section details a set of design goals and methods for achieving the design goals when designing the system configuration for particular installations.

The signalling system configuration shall comply with:

- The ARTC Signalling Engineering Standards & Procedures
- The Ansaldo Microlok II Manuals
- The procedure for Configuration Management during Design, Installation, Testing and Commissioning shall be in accordance with PP-158.

3.2 Design Goals

Traffic levels are important and the higher the traffic the greater the requirements.

3.2.1 High Traffic Areas

Definition

High traffic areas are unidirectional signalling with a headway design of less than 4 minutes or bidirectional signalling with headway design of less than 7 minutes in the normal running direction.

Goals

- Clearly identified safety and reliability requirements and how they are achieved
- Design to ensure independence of each line or minimise impact on adjacent lines

- Common mode failure risks are identified and have a design solution implemented to address the risk.
- Choose equipment with demonstrated level of reliability.
- Provide duplication so that each single failure point will not cause more than one signalling object to fail except for items that can be demonstrated as “unlikely to fail within the expected life of the system”.
- Design to ensure a single failure does not fail more than 2 signals on each line in each direction or have a fall back operational mode that can reduce the impact to equivalent to 2 failed signals in each direction.
- Provide a power supply system with 2 independent sources of supply that will also withstand loss of all incoming power for at least 10 minutes.
- Provide a power supply system that ensures breaks in supply to equipment are normally less that that required to disrupt normal operation of the equipment. Some ancillary equipment may require supply breaks to be less than 20ms.
- All failures within the duplicated system to generate an alarm or warning or be revealed by maintenance tasks.
- Duplicated parts of the system are able to be isolated and have corrective action completed without disruption to train services.
- All new works or alterations within the duplicated part of the system can be undertaken and tested without operational impact except for the final commissioning activities, which are minimised.
- The time delay from power on to the system being fully operational shall be less than 5 minutes.
- Provide facilities to permit disconnection of signalling equipment as per ARTC Signalling Maintenance Procedure SMP 38 Microlok Computer Based Interlocking.

3.2.2 Medium Traffic Areas

Definition

General traffic areas are unidirectional signalling with headway designs of less that 10 minutes or bidirectional signalling with headway designs of less than 15 minutes which do not come within the high traffic area definition.

Goals

- Clearly identified safety and reliability requirements and how they are achieved
- Provide duplication for items that could cause a whole interlocking area to fail.
- Provide duplication for items that may require more than one maintenance team involved in corrective action or will take more than 2 hours to repair.
- Common mode failure risks are identified and managed.
- Choose equipment with demonstrated level of reliability.
- Design to minimise single point failures that can impact on multiple lines.
- Design to ensure a single failure does not fail more than 2 signals on each line in each direction or have a fall back operational mode that can reduce the impact to equivalent to 2 failed signals in each direction.
- Provide a power supply system with 2 independent sources of supply that will also withstand loss of all incoming power for at least 1 minute.
- Provide a power supply system that ensures breaks in supply to equipment are normally less that that required to disrupt normal operation of the equipment.
- All failures within the duplicated system to generate an alarm or warning or be revealed by maintenance tasks.

- Duplicated parts of the system are able to be isolated and have corrective action completed without disruption to train services.
- The time delay from power on to the system being fully operational shall be less than 5 minutes.
- Provide facilities to permit disconnection of signalling equipment as per ARTC Signalling Maintenance Procedure SMP 38 Microlok Computer Based Interlocking.

3.2.3 Low Traffic Areas

Definition

Low traffic areas are all other areas that the High Traffic and General Traffic definitions do not apply.

Goals

- Clearly identified safety and reliability requirements and how they are achieved
- Provide duplication for items that may require more than one maintenance team involved in corrective action.
- Choose equipment with demonstrated level of reliability.
- Provide a power supply system that will prevent a loss of power that will delay more than 1 train under normal circumstances.
- The time delay from power on to the system being fully operational shall be less than 5 minutes.
- Provide facilities to permit disconnection of signalling equipment as per ARTC Signalling Maintenance Procedure SMP 38 Microlok Computer Based Interlocking.

3.3 Failure Modes

The system designer shall consider failure modes due to other equipment, environment ands system configuration. Where appropriate back proving of states of external equipment shall be documented in the design report.

3.4 Type Approval Equipment

Additional Equipment or configurations to protect against failure modes, shall be considered against:

- Common Mode Failure;
- Cascaded Failures
- Comms Links;

4 External Interfaces

There are a number of external interfaces to the Microlok system. These include and are not limited to:

- Track circuit inputs
- Axle counter inputs
- Point detection inputs
- Releases switch inputs
- Other vital indications inputs
- Point control outputs
- Signal LED driver outputs
- Signal incandescent driver outputs
- Other vital control outputs

These interfaces for inputs and outputs to Microlok shall be configured in accordance with ARTC Signals Standards and Engineering Design Notes. Where these do not cover the specific interface or item of equipment, then the Design Manger shall produce a draft Design Note for the specific interface and submit to the ARTC Manager Standards or approval.

4.1 Coded Track Circuits

Interfaces to MicroTrak or other coded track circuits shall address timing and latency of all information. The manner in which this is addressed shall be detailed in the Design Report for the specific installation.

4.2 Interface Timing

The timing of all external interfaces shall be addressed as part of the design process. The result of this analysis shall be detected in the Design Report for the specific installation.

4.3 Interlocking Equipment Configuration

General

Design of Interlocking Equipment Configuration for high traffic areas, general traffic areas and low traffic areas shall be as per ARTC Signal Design Note.

Microlok addresses are to be requested from the ARTC Signal Standards Engineer.

4.4 Control System Communication Link Configuration

General

Received data may need to be conditioned by the link status as the bit status are maintained when the link fails. Communication links must have galvanic isolation between the interlocking equipment and any external circuits. Opto-isolators or transformers are normally used to provide galvanic isolation. Some communications equipment provides galvanic isolation.

Design of Control System Communication Link Configuration for high traffic areas, general traffic areas and low traffic areas shall be as per ARTC Signal Design Note.

4.5 Safety System Communication Link Configuration

General

Safety communication links must not have any buffering or "store and forward" provided in the communications equipment between the Microlok II equipment as per the requirements set out in the Microlok II Platform Safety Application Guidelines.

Typically "dark fibre" or a copper pair is provided and the Fibre Optic Modem arrangements or analogue modems are provided as part of the signalling installation.

Communication links must have galvanic isolation between the interlocking equipment and any external circuits. Opto-isolators or transformers are normally used to provide galvanic isolation. Some communications equipment provides galvanic isolation.

Design of Safety System Communication Link Configuration for high traffic areas, general traffic areas and low traffic areas shall be as per ARTC Signal Design Note.

Microlock Vital Radios links are only to be used in accordance with the approved Design Note.

4.6 Equipment Housing and Cable Route Configuration

General

Equipment housings and cable routes shall comply with specification alterations identified in the Proposal for Standard Specification Alterations to address issues with 415V signalling power distribution, Surge Protection Installation Guidelines and the Ancillary Equipment Temperature Rating Installation Guideline.

Passive temperature control is required on all locations, using a method such as shade structures or double skinning and adequate ventilation.

Siting of any location must consider:

- Protection of the location from damage.
- 1 in 100 year flood.
- Fire risk.
- Surge damage risk.
- Damage due to high voltage power faults.
- Location layout must provide:
- Segregation for wiring and equipment for surge protection.
- Layout of equipment and wiring to minimise coupling of electrical noise onto sensitive circuits.
- Layout of equipment for ease of maintenance.
- Layout of equipment for temperature effects.

Design of Safety System Communication Link Configuration for high traffic areas, general traffic areas and low traffic areas shall be as per ARTC Signal Design Note.

4.7 Power Supply Configuration

General

Power load calculations shall be as per ARTC Signal Design procedure – Signal Power Design.

Power Supply and reticulation design shall consider the requirements for a reliable backed up power supply for the "Red Retaining" function.

Design of Power Supply Configuration for high traffic areas, general traffic areas and low traffic areas shall be as per ARTC Signal Design Note.

The overall power loads of the design configuration including all external interfaces shall be addressed as part of the design process.

4.8 Microlok Specific Configuration Issues

General

Microlok application data must not use look-up tables without specific design guidelines being approved for the particular use.

Microlok application data must not use numeric blocks for purposes other than configuration control without a specific design guideline being approved for the particular use.

External signalling circuits driven by Microlok outputs must not have “stick” paths and Timers without a design review to confirm that short duration “false” outputs do not cause a hazard.

Design of Microlok Configuration for high traffic areas, general traffic areas and low traffic areas shall be as per ARTC Signal Design Note.

4.9 Track Side Equipment Configuration

General

Design of Track Side Equipment Configuration for high traffic areas, general traffic areas and low traffic areas shall be as per ARTC Signal Design Note.

4.10 Cables and Wiring

General

Design of Cable and Wiring Configuration for high traffic areas, general traffic areas and low traffic areas shall be as per ARTC Signal Design Note.

5 Serial Link Communications

5.1 Vital Serial Links

General

All Microlok II vital serial links at each individual site and within each section of the cable route must have a unique serial link address unless they have identical data because they are individual links of a duplicated link arrangement.

If a Microlok II vital serial link is to operate over cabling or communications multiplexing equipment that extends beyond the trackside signalling equipment that an additional 8 bit address must be embedded into the vital serial link data. The application logic must check the additional address and not accept any data unless the address matches the normal address and the additional address.

The Microlok II serial ports have different priorities, port 1 having the highest priority, and port 4 having the lowest priority. Normally the priority of the serial ports will not impact on the design, however if all links are in use and the CPU is heavily loaded it is preferred to allocate the vital links as the lower port numbers.

Design of Serial Link Configuration for high traffic areas, general traffic areas and low traffic areas shall be as per ARTC Signal Design Note.

6 Application Logic Design

6.1 General

The Microlok II development system tools are to be used to develop and compile an application logic program, debug the system and upload the application program to the Microlok II central processing unit (CPU) card.

For comprehensive procedures to create the complete Microlok II application program reference should be made to the US&S Microlok II System Application Logic Programming Guide, SM-6800D manual.

The application logic is to be designed in accordance with the ARTC Signal Design Procedures and agreed Microlok Application Logic Design Standard for the project.

Design Engineers are to ensure the application logic is produced utilising the current approved Microlok II development tools and compilation software.

In general the application logic is based on or derived from the ARTC Signalling Circuit Design Standards. It is important to note all the features that can be programmed into the Microlok II system are not or cannot be part of current relay design methodology. And the features that are part of current relay design methods which are not essential or necessary for the satisfactory operation of computer based interlockings and non-vital equipment.

Typical examples of these are:

- Replication of magnetically latched relays in principle.
- Removal of back contact proving for relay down proving purposes.
- Removal or addition of relay features not relevant to ‘software’ relays.
- Specific maintenance indications and diagnostics.
- Timing and indication features that would be an expensive addition to conventional systems.

Design of Application Logic for high traffic areas, general traffic areas and low traffic areas shall be as per ARTC Signal Design Note.

7 Circuit Design

7.1 General

Consistency between Microlok II applications shall be achieved by designers; in many cases the items are not absolute and if a preferable arrangement is proposed for a specific job approval for the preferred arrangement shall be sought.

Circuit Design for high traffic areas, general traffic areas and low traffic areas shall be as per ARTC Signal Design Note